

Notice of References Cited	Application/Control No. 09/888,856	Applicant(s)/Patent Under Reexamination DANCE ET AL.	
	Examiner Thomas H. Stevens	Art Unit 2121	Page 1 of 2

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,456,894	09-2002	Nulman, Jaim	700/121
*	B	US-6,615,098	09-2003	Bode et al.	700/121
	C	US-			
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Grewal et al., "Integrating Targeted Cycle-Time Reduction into the Capital Planning Process" 1998 Winter Simulation Conference pg. 1005-1010.
	V	Cambell et al., "A Model of a 300mm Wafer Fabrication Line" 1999 Winter Simulation Conference pg. 909-911.
	W	Hallas et al., "An Investigation of Operating Methods for 0.25 Micron Semiconductor Manufacturing" 1996 Winter Simulation Conference. pg.1023-1030.
	X	Robinson et al., "Capacity Planning for Semiconductor Wafer Fabrication with Time Constraints Between Operations" 1999 Winter Simulation Conference pg. 880-887.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Art Unit

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Page 2 of 2

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	U	Domaschke et al., "Effective Implementation of Cycle Time Reduction Strategies for Semiconductor Back-End Manufacturing" Winter Simulation Conference 1998 pg. 985-982.
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